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Docket No.: 500.43446X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Norio HIRAKO
Serial No.:	10/765,109
Filed:	January 28, 2004
For:	STORAGE DEVICE CONTROL APPARATUS AND A METHOD OF CONTROLLING THE SAME
Group:	2188
Special Program Examiner:	Brian Johnson

REQUEST FOR RECONSIDERATION

August 22, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Decision on Petition dated July 20, 2005, reconsideration and withdrawal of the Decision is respectfully requested in view of the following remarks.

REMARKS

Initially, in the Decision on Petition dated July 20, 2005, the Examiner notes that the Petition to Make Special filed June 22, 2005 fails to submit a detailed discussion of U.S. Patent Publication No. 2004/0205294 (Nakayama et al.).

It is submitted that the cited references, whether taken individually or in combination with each other, fail to teach or suggest the invention as claimed. In particular, the cited references, at a minimum, fail to teach or suggest as recited in the claims:

a first feature of the present invention as recited in independent claim 1 wherein the channel controller comprises: a communication interface unit which communicates with the information processor; a data transfer unit connected via a first bus to the communication interface unit for transferring the input/output data communicated between the communication interface unit and the cache memory; and a processor connected via a second bus to the data transfer unit for controlling the data transfer unit; the communication interface unit transmits a read command to the data transfer unit, the read command indicating the processor to read data; and wherein the storage device control apparatus, the data transfer unit does not send, when the first bus conforms to a second communication protocol, the split response to the communication interface unit and sends the read command to the processor; the processor receives the read command, transmits the split response to the data transfer unit, and sends the readout data corresponding to the read command to the data transfer unit; and

the data transfer unit receives the readout data and sends the readout data to the communication interface unit; and

a second feature of the present invention as recited in independent claim 13 wherein the channel controller comprises: a communication interface unit for communicating with the information processor; a data transfer unit connected via a first bus to the communication interface unit for transferring the input/output data communicated between the communication interface unit and the cache memory; and a processor connected via a second bus to the data transfer unit for controlling the data transfer unit, the control method comprising steps of: not sending by the data transfer unit, when the first bus conforms to a second communication protocol, the split response to the communication interface unit and sending the read command to the processor; receiving by the processor the read command, transmits the split response to the data transfer unit, and sending the readout data corresponding to the read command to the data transfer unit; and receiving by the data transfer unit the readout data and sending the readout data to the communication interface unit.

To the extent applicable to the present Petition, Applicants submit that although the distinguishing features may represent a substantial portion of the claimed invention, the claimed invention including said feature(s) and their inter-operation provides a novel storage system and system and method related to or implemented in or by said storage system not taught or suggested by any of the references of record. The distinguishing features may represent a substantial

portion of the claimed invention because the cited references do not teach or suggest any of these limitations.

Further, the cited references fail to teach or suggest the above noted features of the present invention when taken in combination with other limitations recited in each specific claim (e.g., the first feature taken in combination with other limitations recited in claim 1, the second feature taken in combination with other limitations recited in claim 13, etc.).

The references considered most closely related to the claimed invention are briefly discussed below:

U.S. Patent No. 6,219,738 (Kondo et al.) discloses an information processing system which has a bus adapter connected (via processor bus) to processors P1, P2, P3 and main memory 306. A bus adapter 405 initiating a split read access respectively of processors P1, P2 and P3. When a source module initiates a split read access to another module, the source module sends an address of the access destination module and an identifier of the source module. When sending a response to the source module, the destination module returns response data and the identifier of the source module (See e.g., column 1, lines 39-65; column 3, lines 57-66; column 5, lines 11-29; column 7, lines 28-32; Figures 2-9.) However, unlike the present invention, Kondo et al., at a minimum, does not teach or suggest the above described first feature of the present invention as recited in independent claim 1, and the above described second feature of the present invention as recited in independent claim 13.

U.S. Patent Publication No. 2003/0065841 (Pecone) discloses a network storage controller for transferring data between a host computer 14 and a storage device (RAID) 22. At least one channel interface module 42 which is adapted to be connected to the host computer 14 and storage device 22. With a split transaction as supported in PCIX, the device requests the data sends a signal to a target. (See, e.g., Abstract and paragraph 35; Figures 1-4.) However, unlike the present invention, Pecone, at a minimum, does not teach or suggest the above described first feature of the present invention as recited in independent claim 1, and the above described second feature of the present invention as recited in independent claim 13.

U.S. Patent Publication No. 2004/0019713 (Bissessur et al.) discloses a disk controller 554 for controlling disk 560a-560n. The Disk Controller 554 connected to a Bridge 554 and an I/O processor 570 (via bus 572). The Bridge 574 also connected to an External Bus Master 552. The Bridge 574 (with PCI and PCI-X embodiments) may forward read request such as split read requests, out of order with respect to the order in which the requests were made by the original initiator (external bus master 552). If the disk controller 554 responds to a read request received out of the sequential order in which the requests were issued, then the disk controller 554 may return data out of order. The read requests may comprise read requests such as split read requests (sent from the external bus master DMA 556 when processing a descriptor table. (See e.g., Abstract; Paragraphs 40, 42-45, and 53; Figures 2, 6, 10-11, and 13-14). However, unlike the present invention, Bissessur et al, at a minimum, does not

teach or suggest the above described first feature of the present invention as recited in independent claim 1, and the above described second feature of the present invention as recited in independent claim 13.

U.S. Patent Publication No. 2004/0215878 (Takata et al.) discloses a storage device control that includes a channel controller 110 which receives a data input/output request send from information processor 200 to a storage device 300 (see figure 1). A disk controller 140 which controls data input/output operations for the storage device 300. A cache memory 130 which stores input/output data communicated between the channel controller 110 and the disk controller 140. The channel controller 110 comprises a communication interface 111 to communicate with the information processor 200. An input-output controller 114 connected via a first bus to the communication interface unit 111 and cache memory 130. A processor CPU 112 connected via a second bus to the input-output controller 114 for controlling the input-output controller 114. The channel controller 110 accepts block access requests from the information processor 200 according to multiple protocols such as UNIX (NFS 711), Windows (Samba 712), FICON, ESCON, ACONARC or FIBARC protocol. The memory 113 (of channel controller 110) stores a NAS manager 706. The NAS manager 706 which has received a notice (S1913) sends the disk controller 140 a command to instruct to shift to the "split instructions" for a pair of the to-be-copied LU and the to-be-copied-into LU for which a change into the "split state" is specified (S1914, S2214). (See, e.g., Abstract and paragraphs 53, 57, 61, 69, 93, 95, 99, 101-102, 108, 111-112, 126-127, 141-143, 151, and 154; Figures 1,

7-8, 10-11, 18-19, 22, and 25.) However, unlike the present invention, Takata et al., at a minimum, does not teach or suggest the above described first feature of the present invention as recited in independent claim 1, and the above described second feature of the present invention as recited in independent claim 13.

U.S. Patent Publication No. 2004/02025294 A1 (Nakayama et al.) discloses a storage device controlling apparatus which includes: a plurality of channel controllers having a circuit board on which are formed a file access processing section receiving from an information processing apparatus requests to input and output data in files as units via a network and an I/O processor outputting to a storage device I/O requests corresponding to the requests to input and output data; and a disk controller executing input and output of data into and from the storage device in response to the I/O requests sent from the I/O processors, at least one of the channel controllers receives data specifying an assignment of a logical volume to the channel controller, the data being sent from the information processing apparatus, and stores the received assignment. However, unlike the present invention, Nakayama et al., at a minimum, does not teach or suggest the above described first feature of the present invention as recited in independent claim 1, and the above described second feature of the present invention as recited in independent claim 13.

U.S. Patent Publication No. 2005/0050401 (Matsuki et al.) discloses a disk array system that includes a channel control unit 110 which receives a data input/output request send from information processor 200 to a storage device 300 (see figure 1). A disk control unit 140 controls data input/output operations

for the storage device 300. A cache memory 130 which stores input/output data communicated between the channel control unit 110 and the disk control unit 140. The channel control unit 110 comprises a communication interface 111 to communicate with the information processor 200. An input-output control block 114 connected via a first bus to the communication interface block 111 and cache memory 130 (figure 7). A processor CPU 112 connected via a second bus to the input-output control block 114 for controlling the input-output control block 114. The disk control units 140 read data from the storage device 300 under a control of the channel control unit 110. The channel control unit 110 accepts block access requests from the information processor 200 according to multiple protocols such as FICON, ESCON, ACONARC or FIBARC protocol. The channel control unit 110 reads data, which the information processing unit 200 has requested with the Read command, from the cache memory 130. (See, e.g., Abstract, paragraphs 49, 51, 68, 70, 72-73, 98, 101-103, 106, and 113; and Figures 7, 11, 14-16, 22, 24, and 26.) However, unlike the present invention, Matsuki et al., at a minimum, does not teach or suggest the above described first feature of the present invention as recited in independent claim 1, and the above described second feature of the present invention as recited in independent claim 13.

Therefore, since the references at a minimum fail to teach or suggest the above described first feature of the present invention as recited in independent claim 1, and the above described second feature of the present invention as recited in independent claim 13, and further fail to teach or suggest these

features of the present invention in combination with the other limitations recited in each of the specific independent claims, it is submitted that all of the claims are patentable over the cited references.

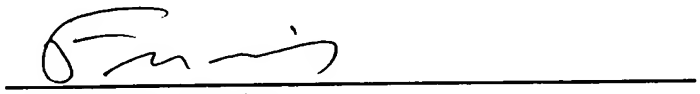
CONCLUSION

Applicant has conducted what it believes to be a reasonable search, but makes no representation that "better" or more relevant prior art does not exist. The Patent Office is urged to conduct its own complete search of the prior art, and to thoroughly examine this application in view of the prior art cited herein and any other prior art that the Patent Office may locate in its own independent search. Further, while Applicant has identified in good faith certain portions of each of the references listed herein in order to provide the requisite detailed discussion of how the claimed subject matter is patentable over the references, the Patent Office should not limit its review to the identified portions but rather, is urged to review and consider the entirety of each reference, and not to rely solely on the identified portions when examining this application.

In view of the foregoing, Applicant requests that this Petition to Make Special be granted and that the application undergo the accelerated examination procedure set forth in MPEP 708.02 VIII.

Respectfully submitted,

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.



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